TS64MLS64V8F2

168PIN PC100 Unbuffered DIMM
512MB With 32MX8 CL2

Description

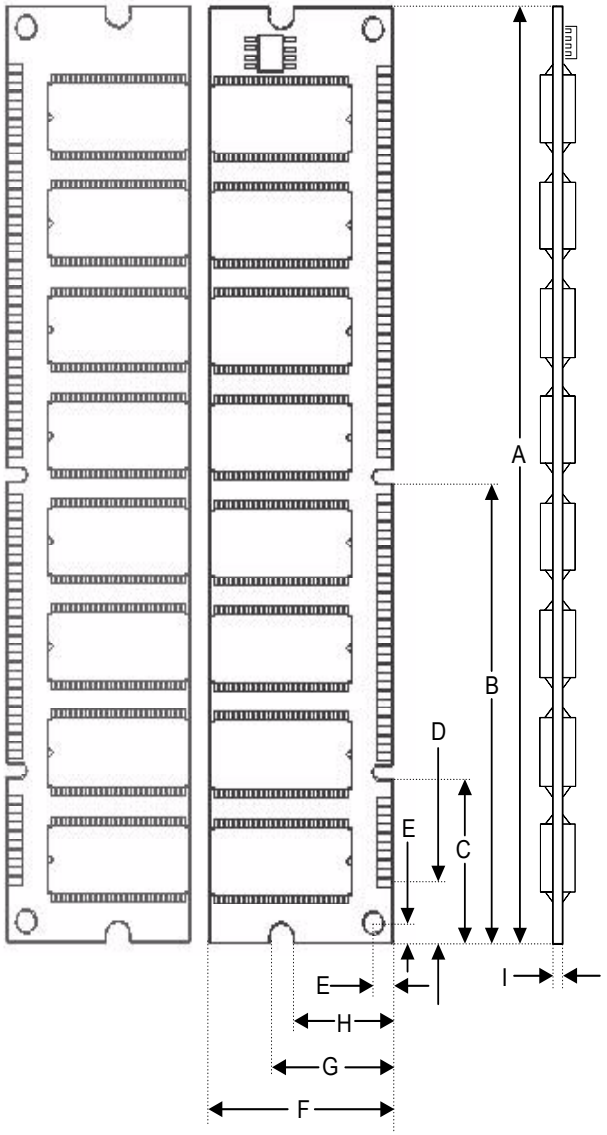
The TS64MLS64V8F2 is a 64M bit x 64 Synchronous Dynamic RAM high-density for PC-100. The TS64MLS64V8F2 consists of 16pcs CMOS 32Mx8 bits Synchronous DRAMs in TSOP-II 400mil packages and a 2048 bits serial EEPROM on a 168-pin printed circuit board. The TS64MLS64V8F2 is a Dual In-Line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Performance Range: PC-100.
- Conformed to JEDEC Standard Spec.
- Burst Mode Operation.
- Auto and Self Refresh.
- CKE Power Down Mode.
- DQM Byte Masking (Read/Write)
- Serial Presence Detect (SPD) with serial EEPROM
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8 & Full Page)
  Data Sequence (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

Placement



PCB:09-7308

Dimensions

Side	Millimeters	Inches
A	133.35±0.40	5.250±0.016
B	65.67	2.585
C	23.49	0.925
D	8.89	0.350
E	3.00	0.118
F	29.21±0.20	1.150±0.008
G	19.80	0.788
H	15.80	0.622
I	1.27±0.10	0.050±0.004

(Refer Placement)

Pin Identification

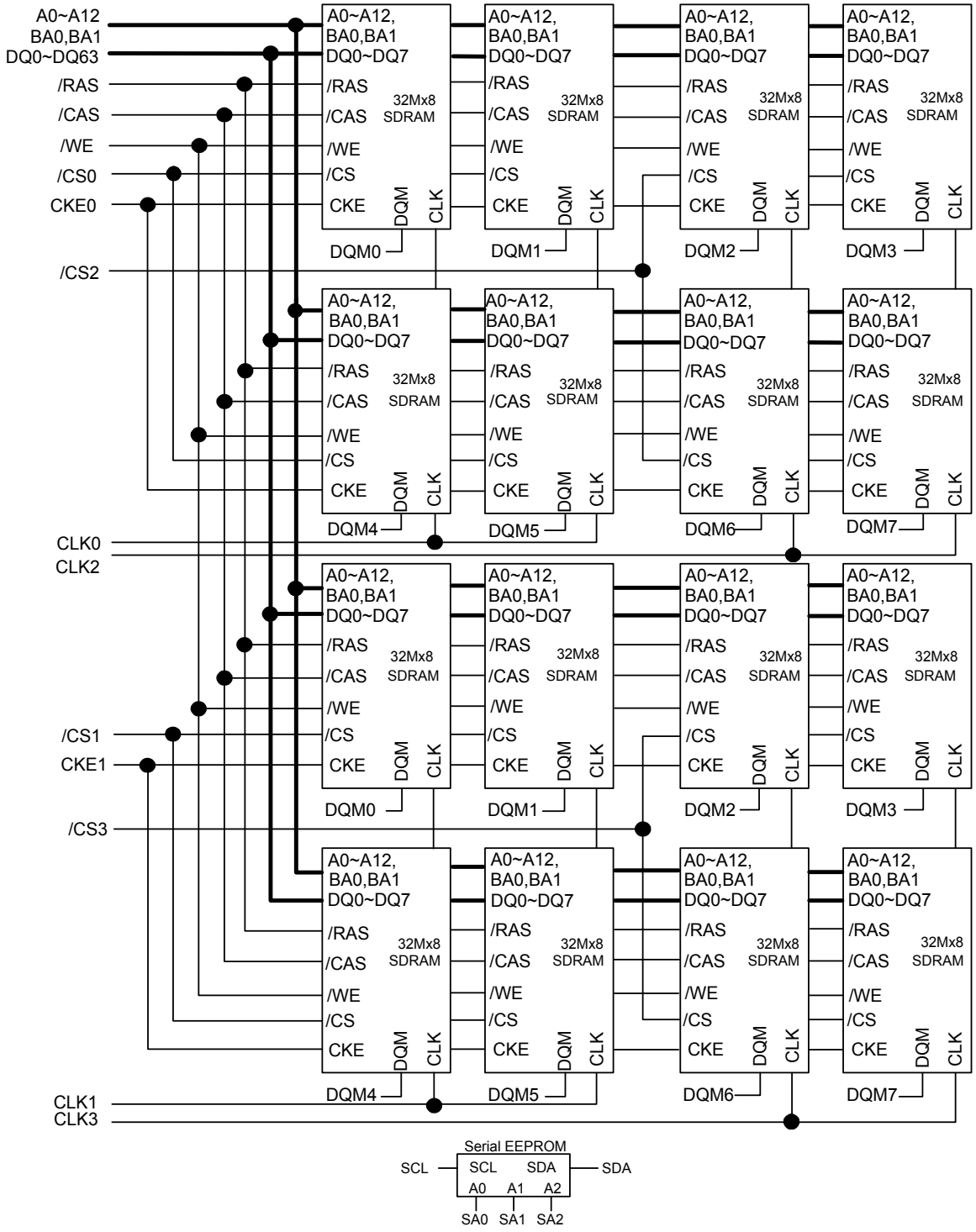
Symbol	Function
A0~A12, BA0, BA1	Address input
DQ0~DQ63	Data Input / Output
CLK0~CLK3	Clock Input
CKE0, CKE1	Clock Enable Input
/CS0~/CS3	Chip Select Input
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQM0~DQM7	Data (DQ) Mask
SA0~SA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
Vcc	+3.3 Voltage Power Supply
Vss	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	43	Vss	85	Vss	127	Vss
02	DQ0	44	NC	86	DQ32	128	CKE0
03	DQ1	45	/CS2	87	DQ33	129	*/CS3
04	DQ2	46	DQM2	88	DQ34	130	DQM6
05	DQ3	47	DQM3	89	DQ35	131	DQM7
06	Vcc	48	NC	90	Vcc	132	*A13
07	DQ4	49	Vcc	91	DQ36	133	Vcc
08	DQ5	50	NC	92	DQ37	134	NC
09	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	*C2	94	DQ39	136	*C6
11	DQ8	53	*C3	95	DQ40	137	*C7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	*Vref	104	DQ47	146	*Vref
21	*C0	63	*CKE1	105	*C4	147	*REGE
22	*C1	64	Vss	106	*C5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	/CS0	72	DQ27	114	*/CS1	156	DQ59
31	NC	73	Vcc	115	/RAS	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	*CLK2	121	A9	163	*CLK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	NC	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	*CLK1	167	SA2
42	CLK0	84	Vcc	126	*A12	168	Vcc

*Please refer Block Diagram

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	IOH=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	IOL=2mA
Input leakage current (Inputs)	I_{IL}	-10	-	10	uA	3
Input leakage current (I/O pins)	I_{IL}	-	-	-	uA	-

Note: 1. V_{IH} (max) = 5.6V AC .The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC .The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (VDD = 3.3V, TA = 20°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0~A_{12}, BA_0~ BA_1)	C_{IN1}	45	85	pF
Input capacitance (/RAS, /CAS, /WE)	C_{IN2}	45	85	pF
Input capacitance (CKE0, CKE1)	C_{IN3}	25	45	pF
Input capacitance (CLK0~CLK3)	C_{IN4}	15	21	pF
Input capacitance (/CS0~/CS3)	C_{IN5}	15	25	pF
Input capacitance (DQM0~DQM7)	C_{IN6}	10	15	pF
Data input/output capacitance (DQ0~DQ63)	C_{OUT1}	13	18	pF

DC CHARACTERISTICS

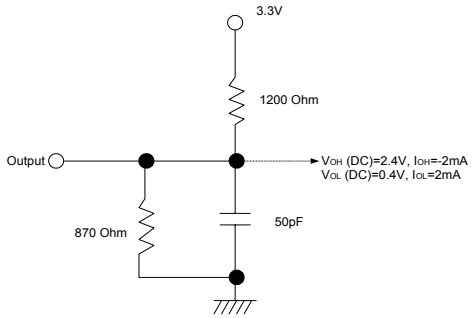
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Value (Typ)	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA	1,120	mA	1
Precharge Standby Current in power-down mode	I_{CC2}**P**	CKE≤V_{IL}(max), t_{CC}=10ns	32	mA	
	I_{CC2}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞	32		
Precharge Standby Current in non power-down mode	I_{CC2}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns	256	mA	
	I_{CC2}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable	224		
Active Standby Current in power-down mode	I_{CC3}**P**	CKE≤V_{IL}(max), t_{CC}=10ns	96	mA	
	I_{CC3}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞	96		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns	480	mA	
	I_{CC3}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable	400		
Operating Current (Bust Mode)	I_{CC4}	I_{OL}= 0 mA Page Burst t_{CCD} = 2CLKs	1,160	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,840	mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V	80	mA	

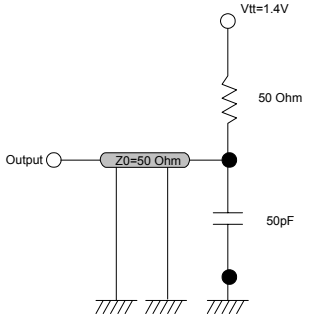
Note: 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V,0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Value	Unit	Note
Row active to row active delay	t_{RRD}(min)	20	ns	1
/RAS to /CAS delay	t_{RCD}(min)	20	ns	1
Row precharge time	t_{RP}(min)	20	ns	1
Row active time	t_{RAS}(min)	50	ns	1
	t_{RAS}(max)	100	us	
Row cycle time	t_{RC}(min)	70	ns	1
Last data in to new col. address delay	t_{CDL}(min)	1	CLK	2
Last data in to row precharge	t_{RDL}(min)	2	CLK	2
Last data in to burst stop	t_{BDL}(min)	1	CLK	2
Col. address to col. address delay	t_{CCD}(min)	1	CLK	3
Number of valid output data		2	ea	4

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter	Symbol	Min	Max	Unit	Note
CLK cycle time	t_{CC}	10	1000	ns	1
CLK to valid output delay	t_{SAC}	-	6.0	ns	1, 2
Output data hold time	t_{OH}	3.0	-	ns	2
CLK high pulse width	t_{CH}	3.0	-	ns	3
CLK low pulse width	t_{CL}	3.0	-	ns	3
Input setup time	t_{SS}	2.0	-	ns	3
Input hold time	t_{SH}	1.0	-	ns	3
CLK to output in Low-Z	t_{SLZ}	1.0	-	ns	2
CLK to output in Hi-Z	t_{SHZ}	-	6.0	ns	

Note:
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)= 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_{12} A_0~A_9	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Note:

1. OP Code: Operand Code
   A_0~A_{12}, BA_0~BA_1: Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at both banks precharge state.
4. BA_0~BA_1: Bank select address.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command cannot be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

SERIAL PRESENCE DETECT SPECIFICATION

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	SDRAM	04
3	# of Row Addresses on this Assembly	13	0D
4	# of Column Addresses on this Assembly	10	0A
5	# of Module Banks on this Assembly	2 bank	02
6	Data Width of this Assembly	64bits	40
7	Data Width Continuation	-	00
8	Voltage Interface Standard of this Assembly	LVTTL3.3V	01
9	SDRAM Cycle Time (highest CAS latency)	10.0ns	A0
10	SDRAM Access from Clock (highest CL)	6.0ns	60
11	DIMM configuration type (non-parity, ECC)	Non parity	00
12	Refresh Rate Type	7.8us/Self Refresh	82
13	Primary SDRAM Width	X8	08
14	Error Checking SDRAM Width	None	00
15	Min Clock Delay Back to Back Random Address	1 clock	01
16	Burst Lengths Supported	1,2,4,8 & Full page	8F
17	Number of banks on each SDRAM device	4 bank	04
18	CAS # Latency	2 & 3	06
19	CS # Latency	0 clock	01
20	Write Latency	0 clock	01
21	SDRAM Module Attributes	Non Buffer	00
22	SDRAM Device Attributes: General	Prec All, Auto Prec, R/W Burst	0E
23	SDRAM Cycle Time (2^{nd} highest CL)	10.0ns	A0
24	SDRAM Access from Clock (2^{nd} highest CL)	6.0ns	60
25	SDRAM Cycle Time (3^{rd} highest CL)	-	00
26	SDRAM Access from Clock (3^{rd} highest CL)	-	00
27	Minimum Row Precharge Time	20ns	14
28	Minimum Row Active to Row Activate	20ns	14

29	Minimum RAS to CAS Delay	20ns	14
30	Minimum RAS Pulse Width	50ns	32
31	Density of Each Bank on Module	1row of 256MB	40
32	Command/Address Setup Time	2.0ns	20
33	Command/Address Hold Time	1.0ns	10
34	Data Signal Setup Time	2.0ns	20
35	Data Signal Hold Time	1.0ns	10
36-61	Superset Information	-	00
62	SPD Data Revision Code	VER 1.2	12
63	Checksum for Bytes 0-62	-	3A
64-71	Manufacturers JEDEC ID Code per JEP-108E	Transcend	7F, 4F
72	Manufacturing Location	T	54
73-90	Manufacturers Part Number	TS64MLS64V8F2	54 53 36 34 4D 4C 53 36 34 56 38 46 32 20 20 20 20 20
91-92	Revision Code	-	0
93-94	Manufacturing Date	By Manufactory	Variable
95-98	Assembly Serial Number	By Manufactory	Variable
99-125	Manufacturer Specific Data	-	0
126	Intel Specification Frequency	100MHz	64
127	Intel Specification CAS# Latency/Clock Signal Support	CL=2, 3 Clock 0~3	F4
128~	Unused Storage Locations	Open	FF